Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

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Claim 1 (Currently Amended): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; [[and]]

a terminal which is formed on the molding resin and is connected to the conductive post[[,]] ~~wherein~~; and

a connecting portion ~~(boundary portion) of~~ between the conductive wiring pattern and the conductive post, the connecting portion having width that gradually decreases toward the conductive wiring pattern,

the connecting portion having ~~is provided with~~ a slit to disperse stress to be applied to the connecting portion.

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Claim 2 (Original): A chip-size semiconductor package according to claim 1, wherein the connecting portion is provided with a plurality of slits, which are separated from each other.

Claim 3 (Currently Amended): A chip-size semiconductor package according to claim 2, wherein the slits are rectangular shaped ~~to be rectangular~~ and are arranged to extend radially away from each other.

Claim 4 (Canceled)

Claim 5 (Currently Amended): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern;

a terminal which is formed on the molding resin and is connected to the conductive post;

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a connecting portion between the conductive wiring pattern and the conductive post; and

a dummy pattern arranged adjacent along sides of the [[a]] connecting portion ~~(boundary portion) of the conductive post and wiring pattern~~.

Claim 6 (Currently Amended): A chip-size semiconductor package according to claim 5, wherein the dummy pattern is a conductive pattern which is formed during a ~~in the~~ same process as the conductive wiring pattern and is arranged parallel to the conductive wiring pattern.

Claim 7 (Currently Amended): A chip-size semiconductor package according to claim 5, wherein the dummy pattern comprises two parts respectively arranged ~~at the~~ along both sides [[side]] of the connecting portion ~~conductive pattern~~.

Claim 8 (Currently Amended): A chip-size semiconductor package according to claim 7, wherein the connecting portion has width that decreases ~~is shaped to decrease in area~~ gradually from the conductive post to the conductive wiring pattern,

the two parts of the dummy pattern are arranged along the conductive post and the conductive wiring pattern.

Claim 9 (Currently Amended): A chip-size semiconductor package, comprising:

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a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; [[and]]

a terminal which is formed on the molding resin and is connected to the conductive post; and

a connecting portion between the conductive wiring pattern and the conductive post, ~~wherein at least one of the conductive wiring pattern and conductive post is provided with~~

wherein a dent is formed at and around [[a]] the connecting portion ~~(boundary portion) of the conductive wiring pattern and conductive post~~.

Claim 10 (Currently Amended): A chip-size semiconductor package according to claim 9, wherein the dent is square shaped ~~to be square~~.

Claim 11 (Currently Amended): A chip-size semiconductor package according to claim 9, wherein the connecting portion has width that decreases ~~is shaped to decrease in~~

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~~area~~ gradually from the conductive post to the conductive wiring pattern.

Claim 12 (Currently Amended): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive wiring pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; [[and]]

a terminal which is formed on the molding resin and is connected to the conductive post; and

a connecting portion between the conductive wiring pattern and the conductive post, ~~wherein~~

the connecting portion having ~~conductive wiring pattern is shaped to have~~ a first region extending outwardly from the conductive post and a second region extending in a perpendicular direction ~~vertically~~ from the first region.

Claim 13 (Currently Amended): A chip-size semiconductor package according to claim 12, ~~wherein the second region comprises~~ further comprising a plurality of projecting

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parts each of which extends in the perpendicular direction ~~vertically~~ from the ~~first region~~ conductive wiring pattern.

Claim 14 (Currently Amended): A chip-size semiconductor package according to claim 13, wherein the ~~projecting pats of the~~ second regions extend ~~region are extended~~ from both sides of the first region.

Claim 15 (Currently Amended): A chip-size semiconductor package according to claim 12, wherein the connecting portion has width that decreases ~~is shaped to decrease in area~~ gradually from the conductive post to the conductive wiring pattern.

Claim 16-17 (Canceled)